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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/590,405 | 10/30/2007 | Franciscus J. Klosters | NL04 0241 US1 | 8682 |

65913 7590 04/08/2009

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| EXAMINER | |
|---|---|
| GUYTON, PHILIP A | |
| ART UNIT | PAPER NUMBER |
| 2113 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 04/08/2009 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/590,405 | KLOSTERS, FRANCISCUS J. | |
| | Examiner | Art Unit | |
| | PHILIP GUYTON | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claim 6 is objected to because of the following informalities: the phrase "bringing an electronic circuit arrangement in a pre-defined state" is grammatically incorrect.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 7,089,462 to Floyd et al. (hereinafter Floyd).

With respect to claim 1, Floyd discloses an electronic circuit arrangement comprising:

a clock fail circuit (figure 2, item 40 – clock fault detector) arranged to receive a clock signal and to generate an error signal upon an absence of the clock signal (column 3, lines 29-35); and

an asynchronous processor (figure 1, items 30 and 34A-B and column 1, lines 25-35) arranged to receive said error signal and to bring the electronic circuit

arrangement into a pre-defined state upon detection of the error signal (column 3, lines 35-46).

With respect to claim 2, Floyd discloses in that the asynchronous processor comprises an interrupt input for receiving the error signal and is further arranged to execute software instructions upon reception of the signal (column 3, lines 32-46).

With respect to claim 3, Floyd discloses an integrated circuit comprising an electronic circuit arrangement as claimed in claim 1 (figures 1-3).

With respect to claim 4, Floyd discloses a bus station for use in a bus system comprising an electronic circuit arrangement as claimed in claim 1 (figure 1).

With respect to claim 6, Floyd discloses a method for bringing an electronic circuit arrangement in a predetermined state, the method comprising:

detecting an absence of a clock signal using a clock fail circuit (column 3, lines 29-32 and figure 2, item 40 – clock fault detector);

generating an error signal in response to the absence of the clock signal (column 3, lines 29-35); and

bringing the electronic circuit arrangement into the pre-defined state (column 3, lines 35-46) using an asynchronous processor within the electronic circuit arrangement (figure 1, items 30 and 34A-B and column 1, lines 25-35).

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Floyd in view of U.S. Patent No. 6,959,014 to Pohlmeyer et al. (hereinafter Pohlmeyer).

Floyd does not disclose expressly wherein the bus station is a bus station for use in a LIN bus system.

However, Pohlmeyer teaches determination of synchronization between transmitters and receivers in a LIN bus system (abstract and column 1, lines 12-27).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Floyd for use on a LIN bus system, as taught by Pohlmeyer. A person of ordinary skill in the art would have been motivated to do so because it is necessary to retain synchronization between nodes in a LIN bus system, as disclosed by Pohlmeyer (column 1, lines 22-27). Thus, loss of clock, or clock error would be highly detrimental in a LIN bus system (Pohlmeyer – column 2, lines 41-49 and column 4, lines 1-15). Floyd teaches a multiprocessor bus system with clock fault determination (column 1, lines 25-35), which would have been highly integratable with the LIN bus system of Pohlmeyer, which is also a multiprocessor bus system (column 2, lines 62-64).

## ***Response to Arguments***

6. Applicant's arguments filed 19 December 2008 have been fully considered but they are not persuasive. Applicant argues Floyd does not disclose “an asynchronous

processor arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal," as recited in amended claim 1. More specifically, applicant states Floyd does not disclose that the service processors 34A-B are involved in actions that occur in response to a clock fault output signal assertion (column 3, lines 35-40). The examiner respectfully disagrees. Floyd teaches wherein the clock fault output signal is provided to control logic within processor 30 and may be provided to service processors 34A-B (column 3, lines 32-35). Floyd further teaches, "[**i**]**n response to clock fault output signal assertion**, a variety of actions may be taken, including stopping processor 10, stopping the entire multiprocessing system (checkstop), and/or isolating processor group 5 from other processor groups" (column 3, lines 35-40). In other words, the disclosed variety of actions are taken by the processor 30 or service processors 34A-B in response to receiving the clock fault output signal. Therefore, Floyd effectively teaches an asynchronous processor arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal, as recited in the claim. Applicant applies identical arguments to claim 6, and therefore claim 6 is taught by Floyd for at least the same line of reasoning.

## ***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHILIP GUYTON whose telephone number is (571) 272-3807. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Philip Guyton/
Examiner, Art Unit 2113
4/3/09

/Robert W. Beausoliel, Jr./
Supervisory Patent Examiner, Art Unit 2113